Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Source connection centrally between indicator lines: .057” Mils**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: Gate .020” X .025”**

**Backside Potential: Drain**

**Mask Ref: HEX 2.5 GEN 5**

**APPROVED BY: DK DIE SIZE .110” X .140” DATE: 8/30/21**

**MFG: IR THICKNESS .019” P/N: IRLC044**

**DG 10.1.2**

#### Rev B, 7/19/02